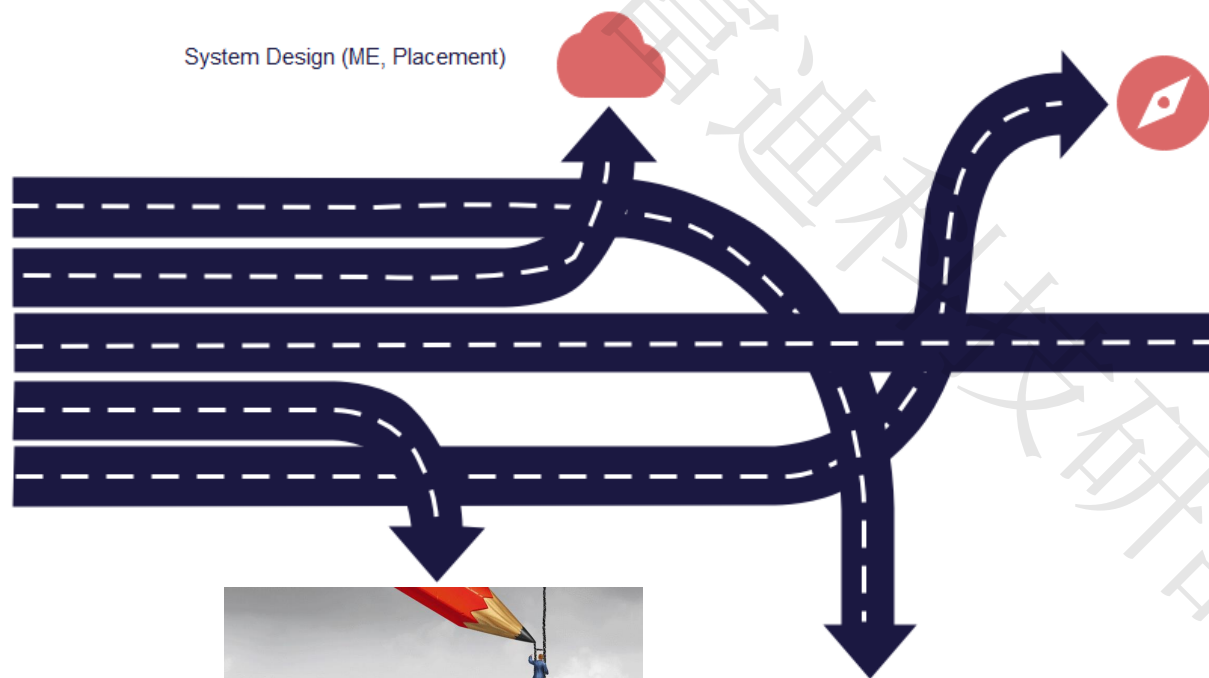


Worthless Thermal Simulation?

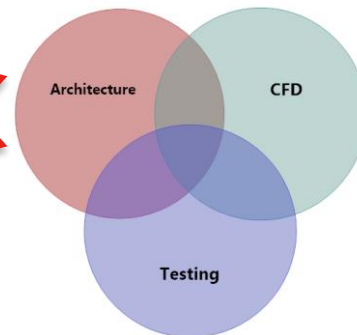
Hank Chung
v1 – 2019/11/8



Product Develop Route



Professional

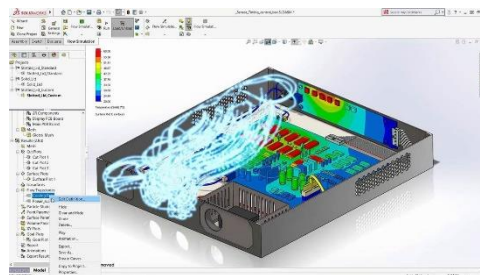


Win Business

Failed results
(architecture)



Independent design route
(Long lead time)



Wrong results (inputs, BCs)

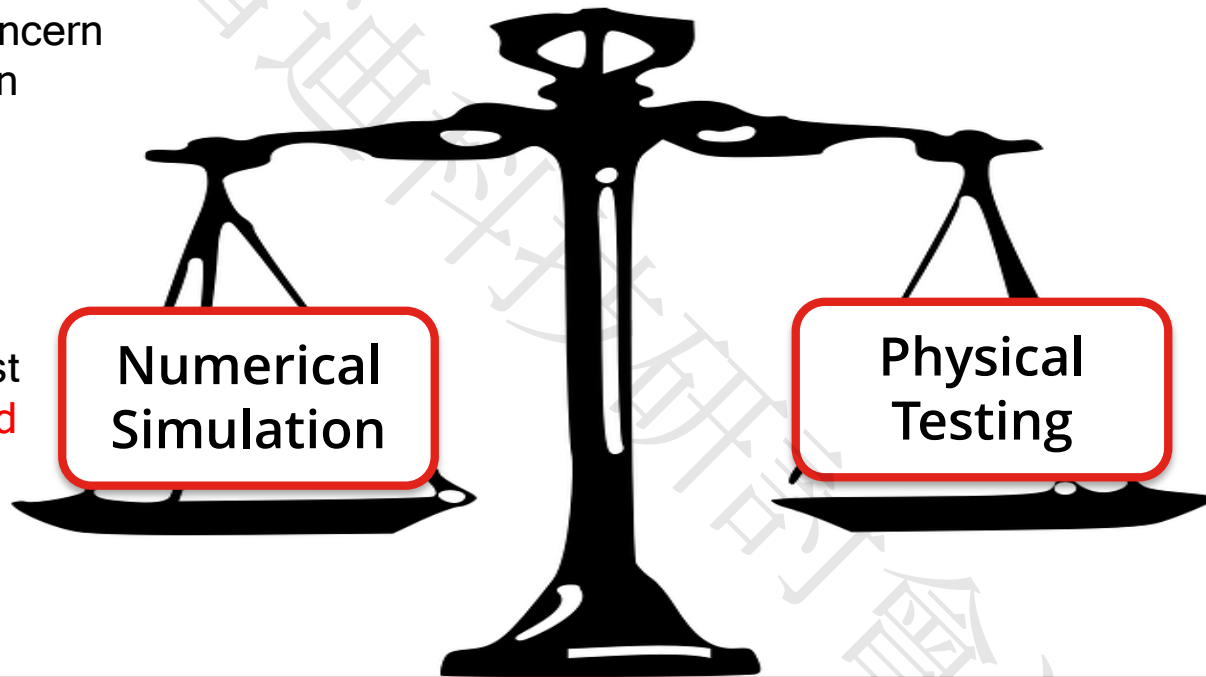
Which is more important?

☆ Ideal

- No GRR concern
- Visualization

☆ Cheap

- Mockup cost
- Experienced CFDer
- Software



☆ Real

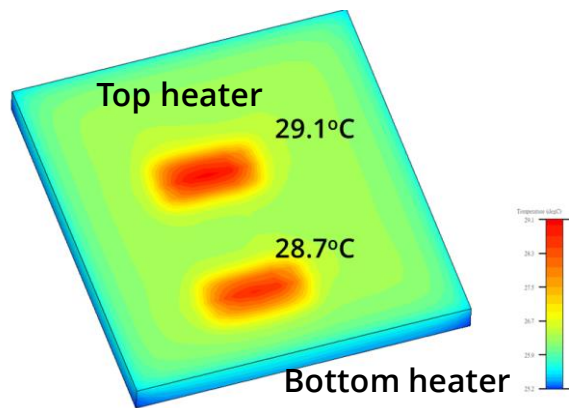
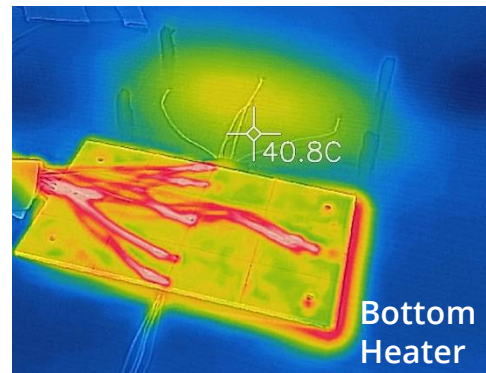
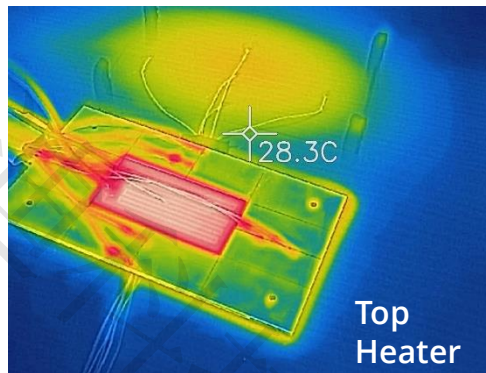
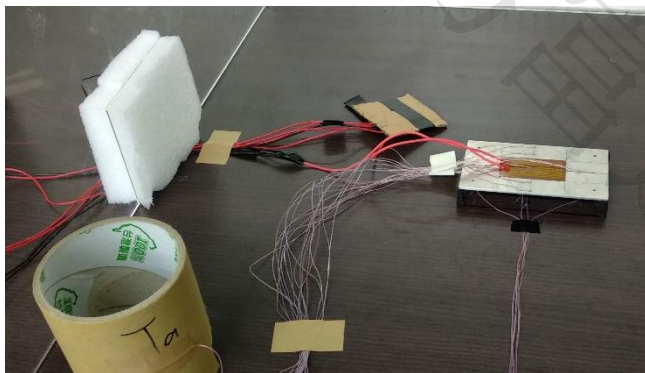
- P-Q
- TIM
- Power consumption
- Bypass flow

☆ Quick

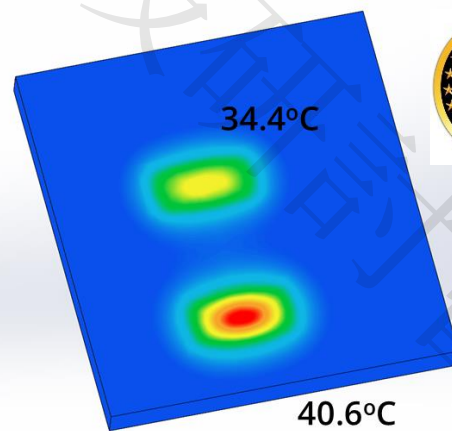
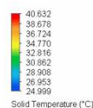
- Push start
- Technician
- Thermal resistance

- Solve thermal **issue** is the most important
- Ability to provide solution quickly and **exactly**

Radiation Performance Check



FloTHERM 12.2

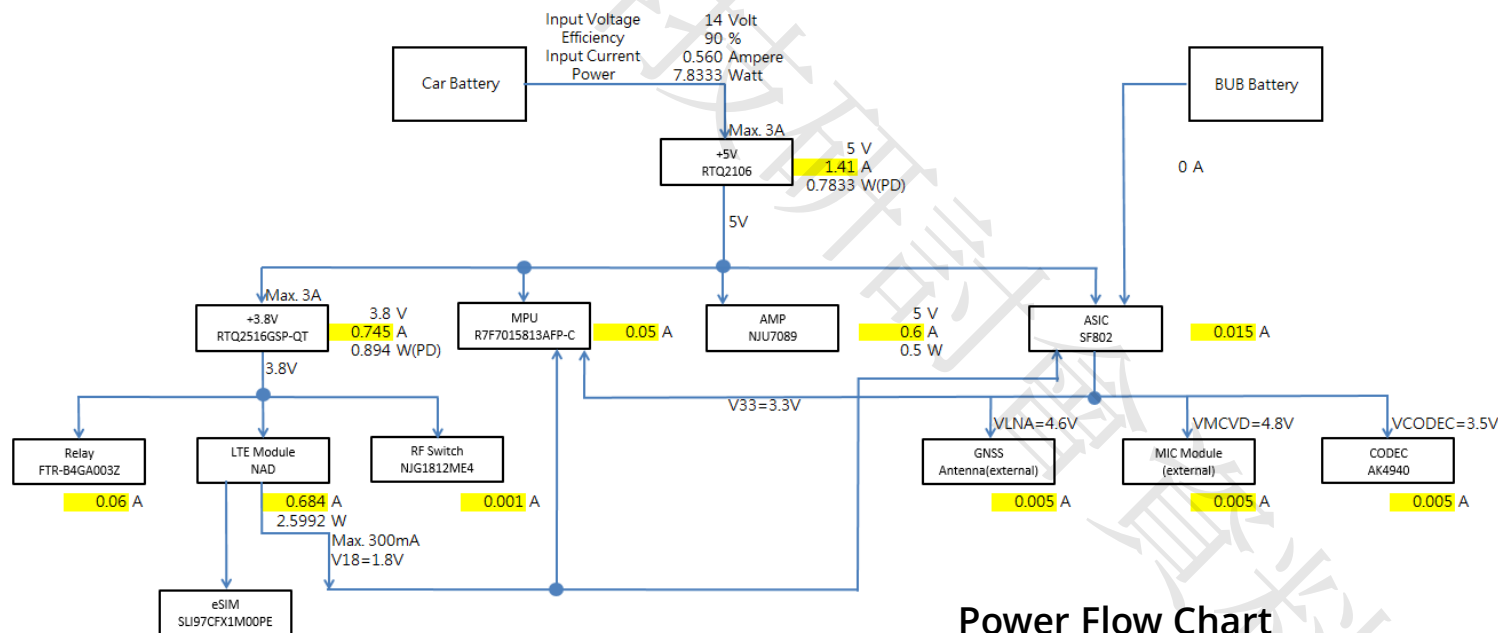


FloTHERM XT 3.3

Table temperature	Top Heater	Bottom Heater
FT@25°C	29.1	28.7
XT@25°C	34.4	40.6
Test	30.9	38.7
Ambient	24.1	23.9
Test @25°C	31.8	39.8

How Heat Generated?

- How to calculate the real heat dissipation?
 - Joule's Law: $P=V \cdot I$
 - Waste heat: $Q_{\text{loss}}=Q_{\text{in}}-Q_{\text{out}}$



Power Flow Chart

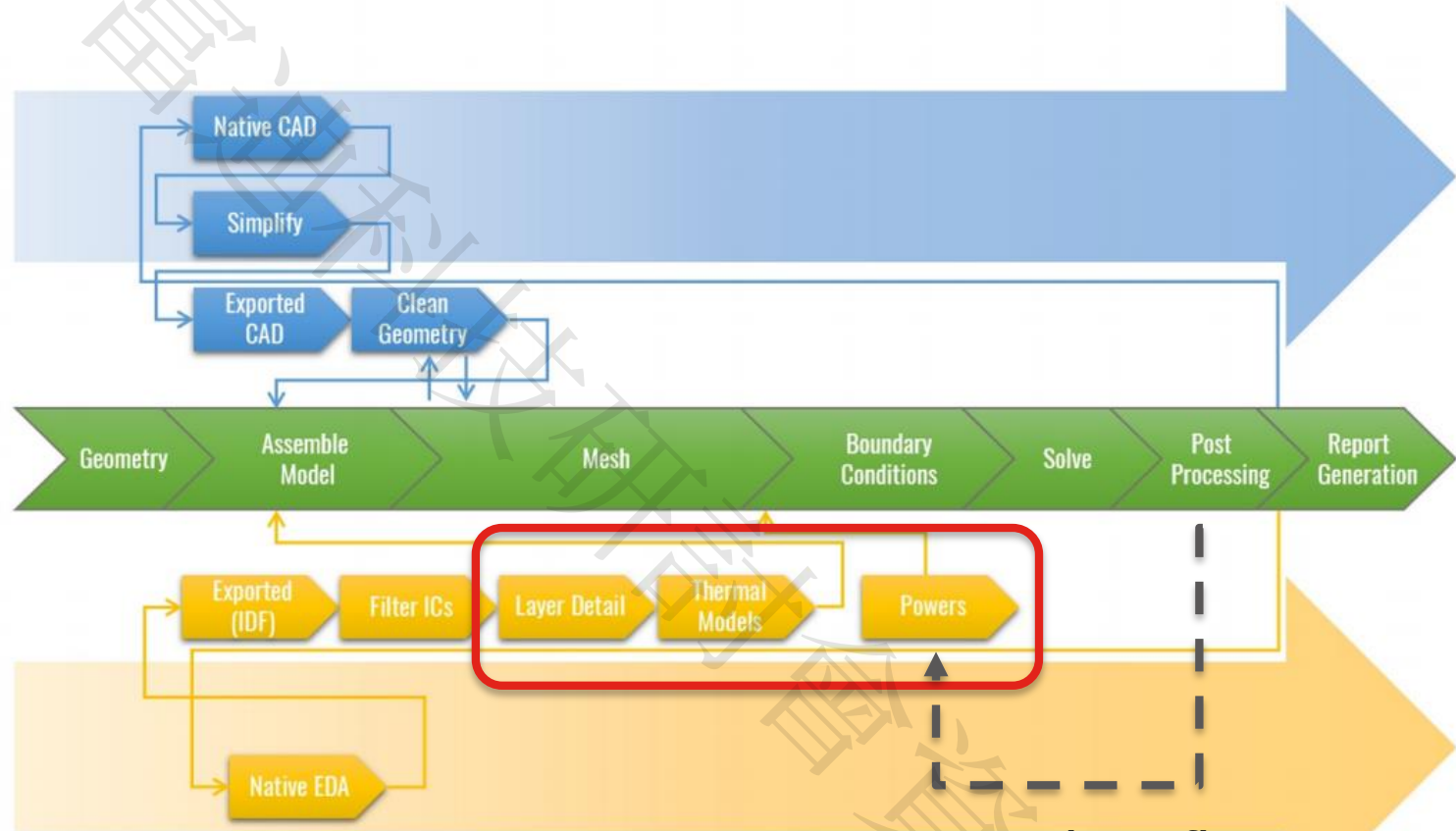
Traditional CFD Flow Chart

COMPRESSING THE THERMAL DESIGN PROCESS



- Foresight
- Insight
- Optimize

MDA Design Flow

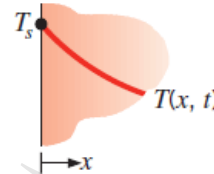


Constant heat flux →
Constant temperature

Thermal Boundary Conditions

1. Constant surface temperature

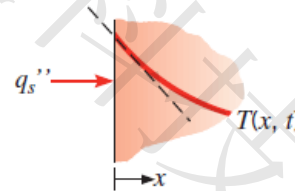
$$T(0, t) = T_s \quad (2.31)$$



2. Constant surface heat flux

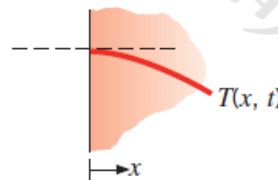
- (a) Finite heat flux

$$-k \frac{\partial T}{\partial x} \Big|_{x=0} = q_s'' \quad (2.32)$$



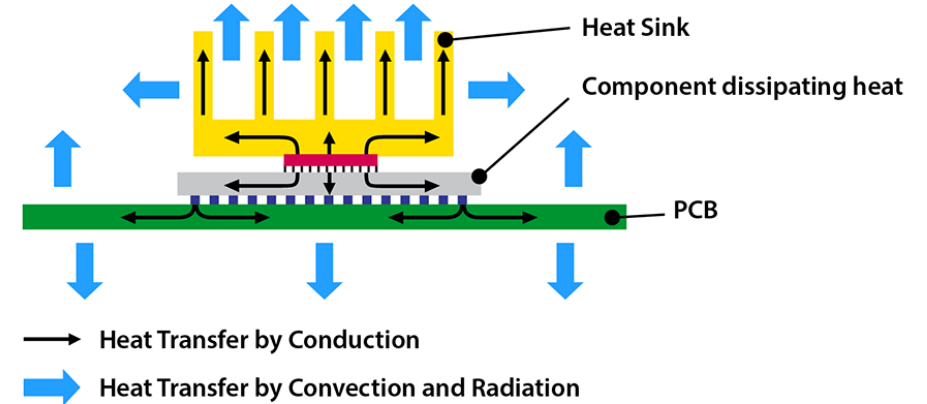
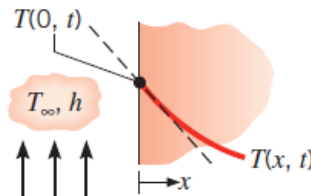
- (b) Adiabatic or insulated surface

$$\frac{\partial T}{\partial x} \Big|_{x=0} = 0 \quad (2.33)$$



3. Convection surface condition

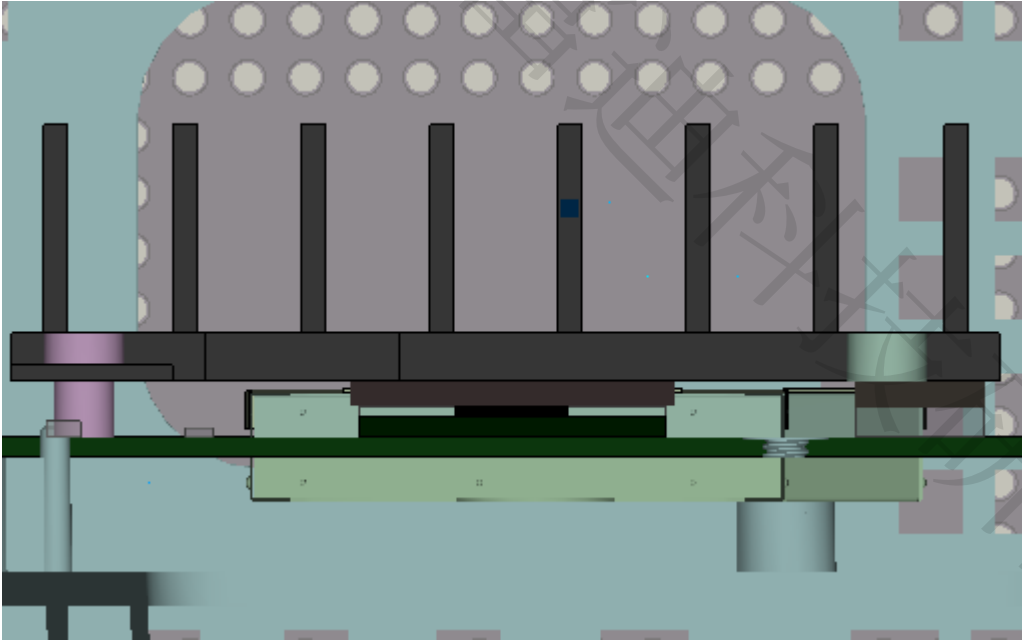
$$-k \frac{\partial T}{\partial x} \Big|_{x=0} = h[T_\infty - T(0, t)] \quad (2.34)$$



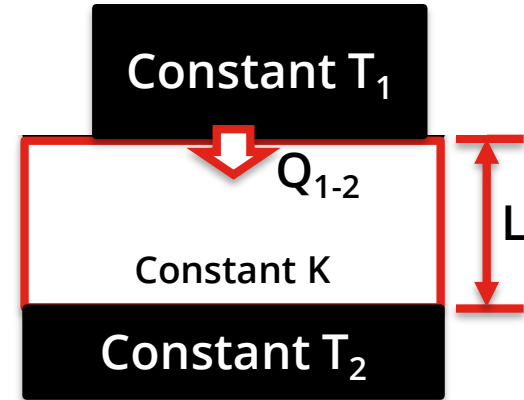
Given total heat, calculate temperature

Known temperature, calculate the heat dissipation

Scenario 1



Ex:
Thermal PAD

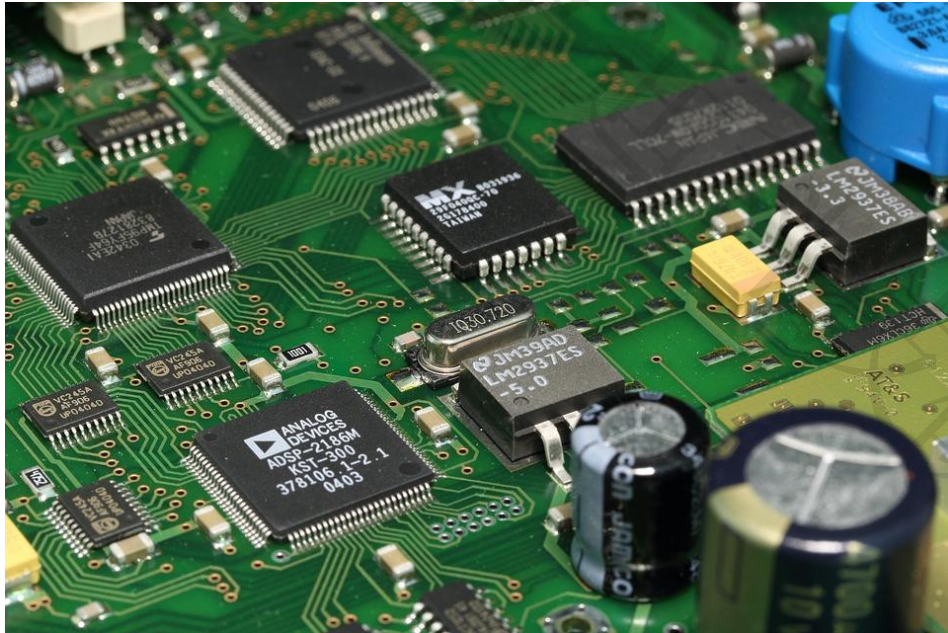


- Fourier's law

$$Q_{1-2} = KA_1 \frac{T_1 - T_2}{L}$$

$$Q = -KA\nabla T$$

Scenario 2



Ex:
PCB, IC Package (Network, Detail model)

Constant T_1

Constant T_2

$Q_{1-2} = ?$

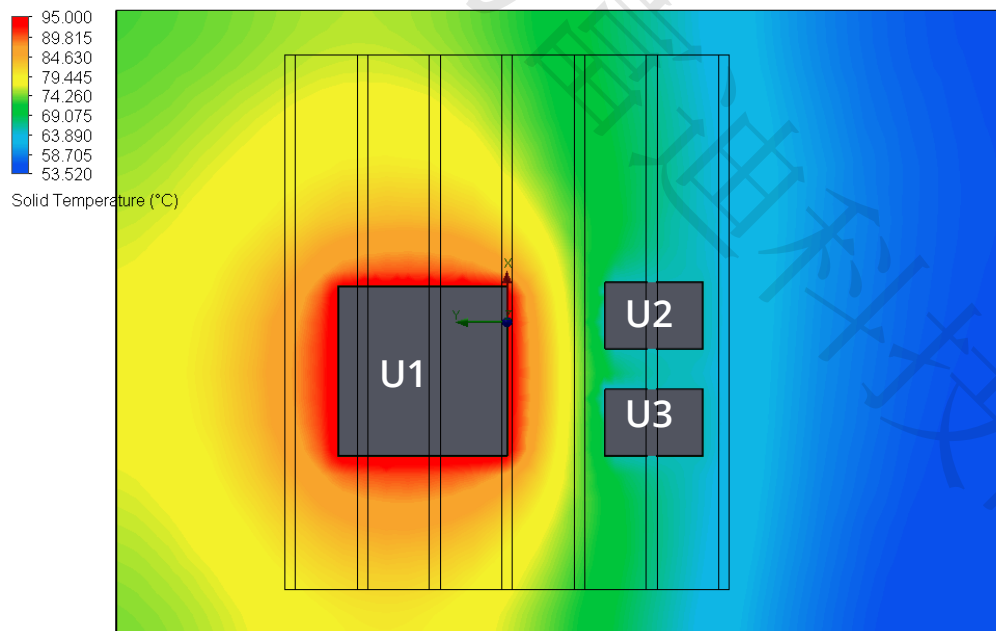


Constant T_1

Constant K

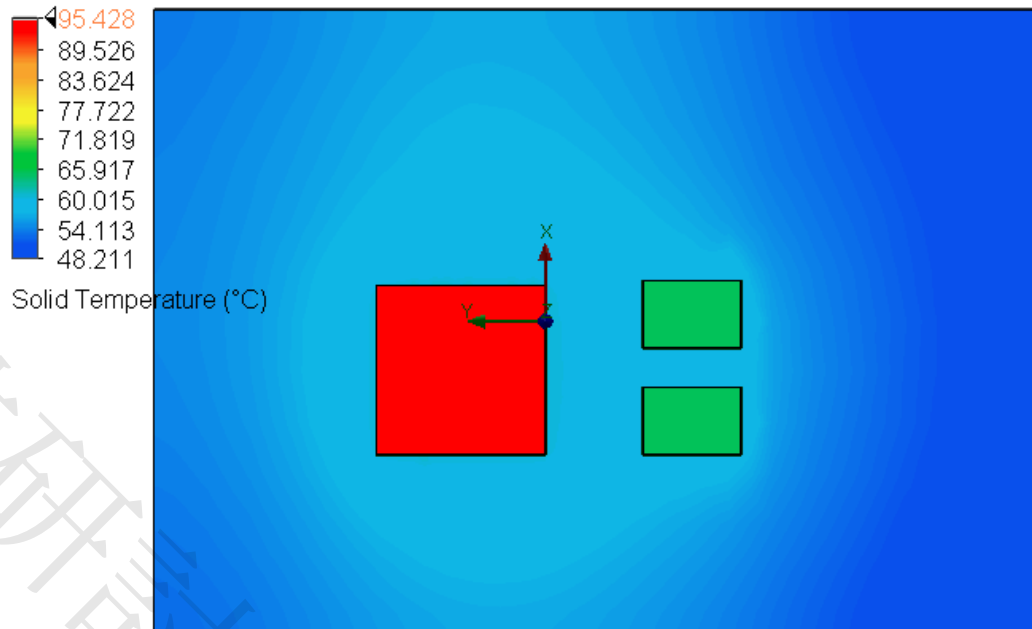
$Q_{1-2} = Q_{out}$

Example



#1	U1	U2	U3
T_{case}	85	70	70
Power	15.2165	0.09911	0.13282

#2	U1	U2	U3
T_{case}	95	65	65
Power	20.4081	-1.283	-1.3956



#3	U1	U2	U3
T_{case}	95	65	65
Power	13.5	0.5	0.5
R_{jc} (K/W)	0.1	5.6	5.6
R_{jb} (K/W)	20	12.6	12.6

PCB Layer

Modeling Level

Modeling Level

Thermal Conductivity Calculation

Calculation Type

Material

Type

Layer Definition

Layers

Signal_1

Conductor Material

Dielectric Material

Summary

Axial Conductivity

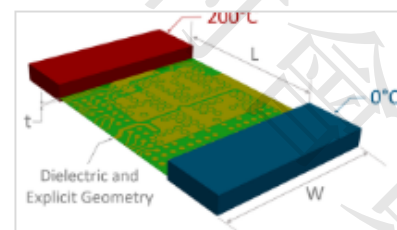
In Plane Conductivity

Effective Density

Effective Specific Heat

Conducting Layers

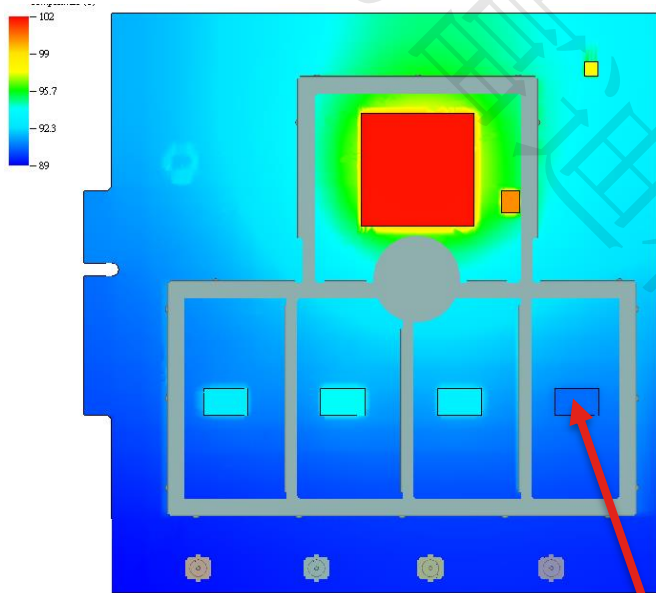
	Layer	Thickness	% Cover	Conductor	Dielectric
	Signal_1	0.017 mm	80	Copper	FR4
	Dielectric_2	4.48918 Oz	1	Copper	FR4
	Power_3	0.034 mm	90	Copper	FR4
	Dielectric_4	4.48918 Oz	1	Copper	FR4
	Signal_5	0.017 mm	80	Copper	FR4
	Dielectric_6	4.48918 Oz	1	Copper	FR4
	Signal_7	0.017 mm	80	Copper	FR4
	Dielectric_8	4.48918 Oz	1	Copper	FR4
	Power_9	1 Oz	90	Copper	FR4
	Dielectric_10	4.48918 Oz	1	Copper	FR4
	Signal_11	0.5 Oz	80	Copper	FR4



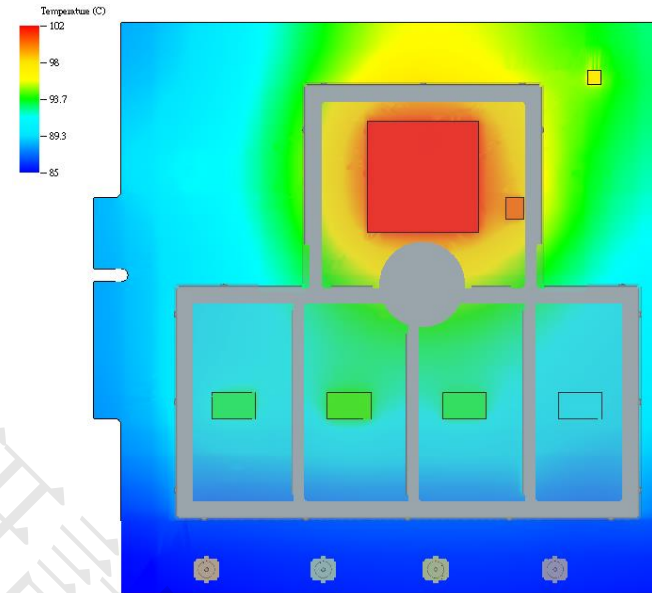
**PCB Thermal Modeling with
Empirical Thermal
Conductivity Methods**

WHITE PAPER

Material Impact



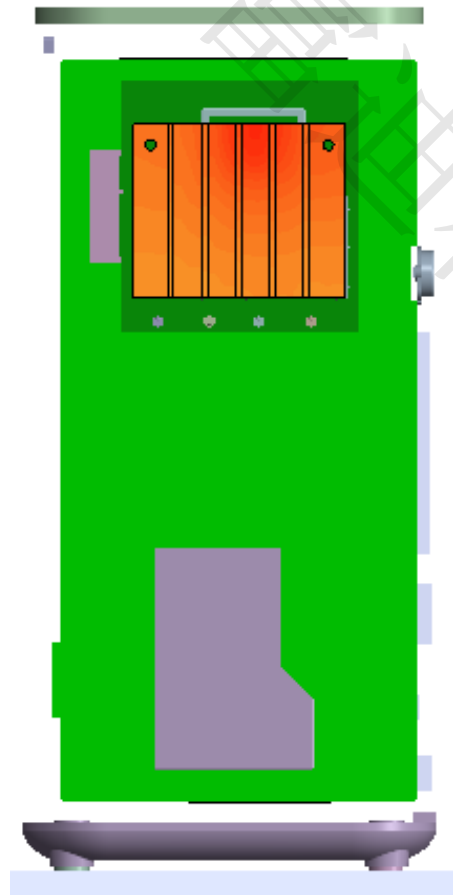
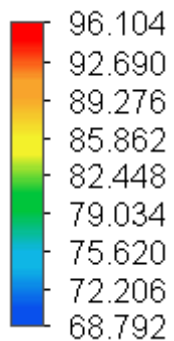
PCB $K_x=K_y=111\text{W/mK}$
 $K_z=0.468\text{W/mK}$



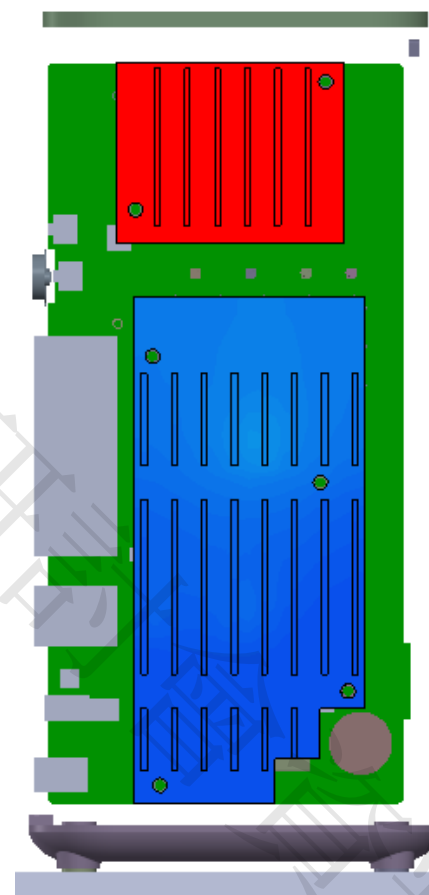
PCB $K_x=K_y=20\text{W/mK}$
 $K_z=5\text{W/mK}$

- IC temperature lower than PCB → IC become heatsink
- Surface data inspector value is negative

Sink Temperature



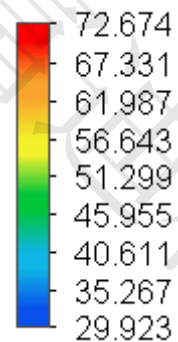
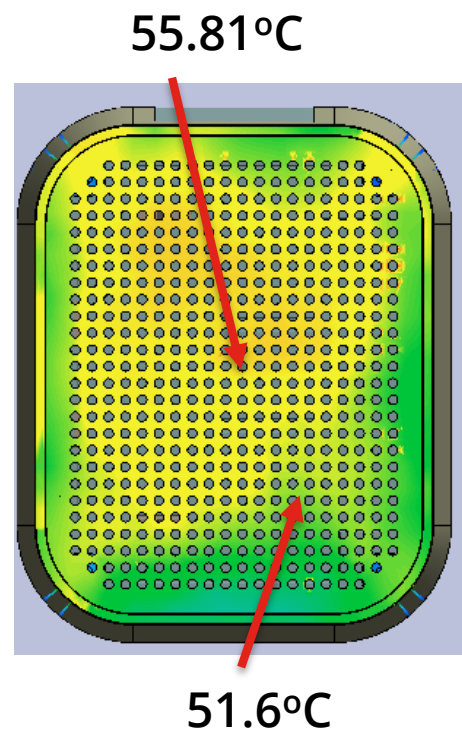
93.4°C/
Tested
95.9°C



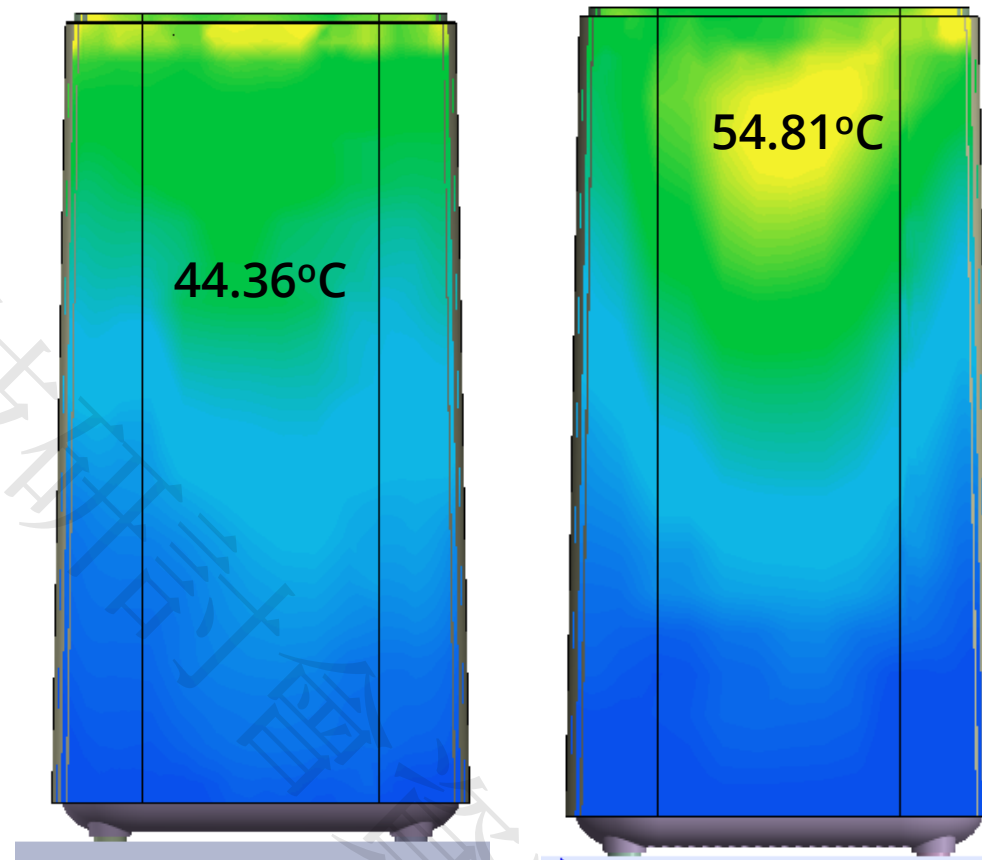
95.2°C/
Tested
95.39°C

72.56°C/
Tested
73°C

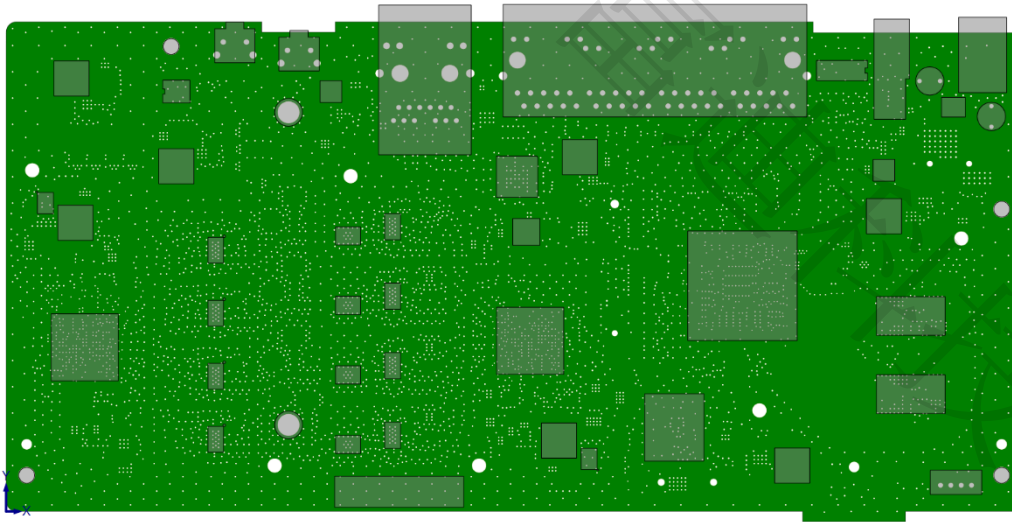
Chassis Temperature



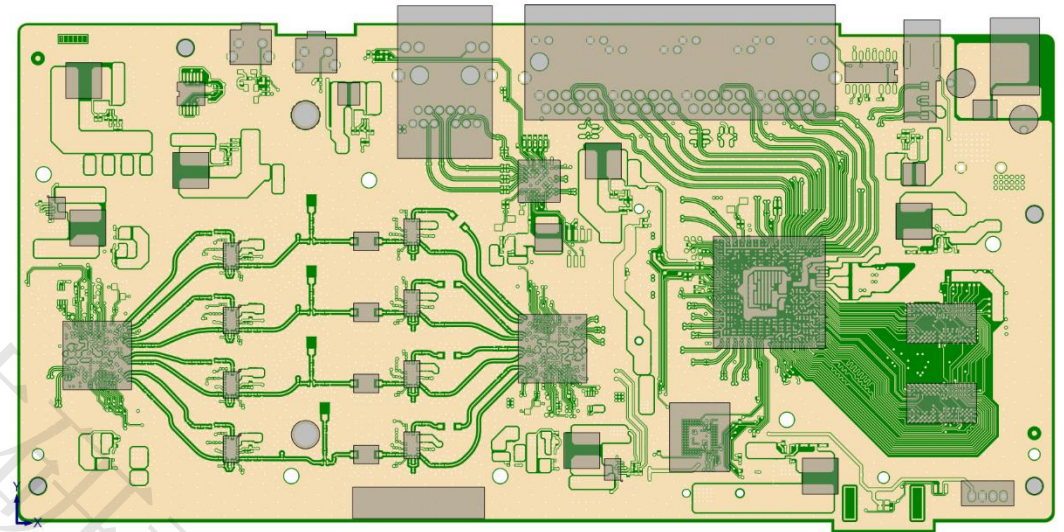
Top(hot)	55.45
Top	52.11
Left	44.32
Right	53.10
Ta	26.37



Import EDA Data



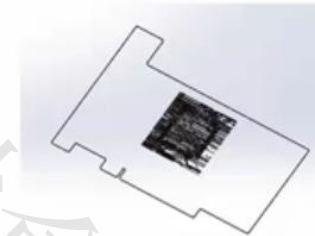
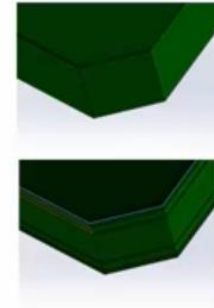
Layer Details	
Name	dielectric_1
Thickness	4.72 mil
Dielectric Material	FR4
Conducting Material	Copper
% Cover	3.26352



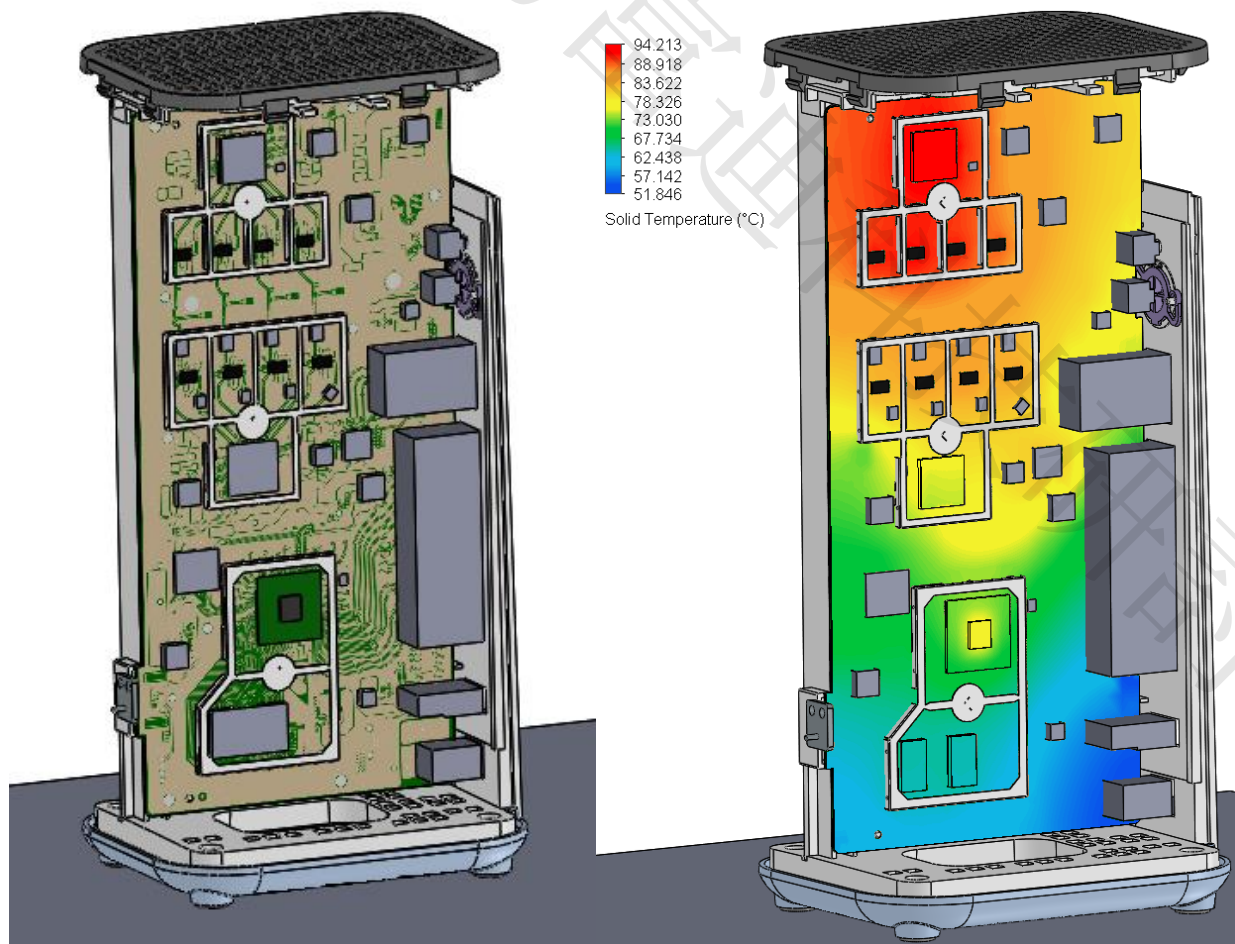
Layer Details	
Name	l1-top-
Thickness	1.65 mil
Dielectric Material	FR4
Conducting Material	Copper
% Cover	79.62568

FloEDA

- Currently the copper from imported boards is modelled as:
 - Compact board – single block with in plane and through plane conductivity.
 - Detailed board – individual layers with copper “smeared” over whole board.
 - Thermal Territory – explicit copper in component footprint.
 - Explicit copper nets – whole electrical net modelled in detail.



PCB Setting



Modeling Level
Modeling Level: **Detail**

Thermal Conductivity Calculation
Calculation Type: **Analytical**

Material
Type: **Layer Definition**

Layer Definition
Layers: **l1-top-**

Conductor Material: **Copper**

Dielectric Material: **FR4**

Summary
Axial Conductivity: 318.84 W/(m K)
In Plane Conductivity: 318.84 W/(m K)
Effective Density: 7379.0 kg/m³
Effective Specific Heat: 401.72 J/(kg K)
Conducting Layers: 6

Modeling Level
Modeling Level: **Compact**

Thermal Conductivity Calculation
Calculation Type: **Analytical**

Material
Type: **Layer Definition**

Layer Definition
Conductor Material: **Copper**

Dielectric Material: **FR4**

Summary
Axial Conductivity: 15.550 W/(m K)
In Plane Conductivity: 51.282 W/(m K)
Effective Density: 2338.4 kg/m³
Effective Specific Heat: 585.97 J/(kg K)
Conducting Layers: 6

Layer Definition
Layer: **l1-top-**

Layer	Thickness	% Cover	Conductor	Dielectric
l1-top-	1.65 mil	79.6268	Copper	FR4
dielectric_1	4.72 mil	3.26352	Copper	FR4
l2-gnd-	1.3 mil	91.72443	Copper	FR4
dielectric_2	4.8 mil	3.26352	Copper	FR4
l3-vec-	0.65 mil	86.11294	Copper	FR4
dielectric_3	22.41 mil	3.26352	Copper	FR4

	Grid Number	CPU Time
Detail Model	574,107	30min18s
Compact Model	552,679	25min13s

Q & A

易普迪科技(香港)有限公司

Thank you!



Manufacturing Experiences.

Since 1989.